Abstract

Network-on-Chip has been proposed as a viable solution to counter the inefficiency of buses in the current VLSI on-chip interconnects. However, as the silicon chip accommodates more transistors, the probability of transient faults is increasing; making fault tolerance is a key concern in scaling chips. In packet based communication on a chip, transient failures can corrupt the data packet and hence, undermine the accuracy of the data communication.

This work examines error detection schemes in the network-on-chip domain. A new encoding scheme "Error Detection by Counting" is designed and a comparative analysis is made among simple parity check, cyclic redundancy check, repeated bit method and error detection by counting. A (4x4) mesh on-chip network was simulated to get the experimental results. By the results the reliable packet delivery of Interlock Parity Check was found to be 81.11% quite higher than other encoding techniques. This proposed scheme consumed less clock cycles as compared to encoding techniques mentioned above. More over average throughput of network traffic with new proposed technique has improved by 20% to 25%.

This work provides network-on-chip designers a reliable error detection scheme for future on-chip designs. This new technique is easy and cheap to implement and this is first attempt to investigate encoding techniques. The effectiveness of the proposed error detection scheme has been validated by NetCount simulator.